IN THE TITLE:

Please delete the title as filed and replace it with the following new title:

--SEMICONDUCTOR DEVICE HAVING AN INSULATION FILM WITH REDUCED WATER CONTENT--.

IN THE SPECIFICATION:

Please amend the specification as follows:

Page 16, line 29, change "FIG. 5" to FIG. 4--.

Page 17, line 5, change "FIG. 10" to --FIG. 11--;

Page 17, line 15, change "FIG. 10" to --FIG. 9--.

IN THE CLAIMS:

Please **CANCEL** claims 30, 32, 36 and 41 without prejudice or disclaimer of the subject matter recited therein.

Please **AMEND** the claims to read as follows:

28. (Amended) A semiconductor device, comprising:

a substrate;

a gate electrode provided on said substrate;

a diffusion region formed in said substrate adjacent to said gate electrode;

a side-wall insulation film formed on a side wall of said gate electrode; [and]

a self-aligned contact hole defined by said side-wall oxide film and exposing said diffusion region; and

a silicide region formed selectively on a surface of said diffusion region;

wherein said semiconductor device further includes;

a first insulation film provided on said gate electrode so as to cover said side wall oxide film partially;

a second insulation film having a composition different from a composition of said first insulation film and provided on said first insulation film;

an interlayer insulation film deposited on said second insulation film;

a contact hole formed in said interlayer insulation film, said contact hole extending through said first and second insulation films and exposing said self-aligned contact hole;

said first insulation film contacts H_2O with an amount smaller than about 2.4 wt%.

31. (Amended) A semiconductor device as claimed in claim 28, further comprising a conductor pattern contacting with said diffusion region and said gate electrode such that said conductor pattern extends [between said side wall oxide film and said first insulation film] along a surface of said side wall oxide film.

33. (Amended) A semiconductor device as claimed in claim [32] 28, further comprising [a] another silicide [layer] region formed selectively on a surface of said [ate] gate electrode.

34. (Amended) A semiconductor device, comprising:

a substrate;

a gate electrode provided on said substrate;

a diffusion region formed in said substrate adjacent to said gate electrode;

a side-wall insulation film formed on side wall of said gate

a side-aligned contact hole defined by said side-wall oxide film and exposing said diffusion region; and

a silicide region formed selectively on a surface of said diffusion region,

wherein said semiconductor device further includes:

a first insulation film provided on said gate electrode so as to cover said side wall oxide film partially;

a second insulation film having a composition different from a composition of said first insulation film and provided on said first insulation film;

an interlayer insulation film deposited on said second insulation film;

a contact hole formed in said interlayer insulation film, said contact hole extending through said first and second insulation films and exposing said self-aligned contact hole;

said first insulation film is formed of PSG containing P with an amount of about 6 wt% or less.

35. (Amended) A semiconductor device as claimed in claim 34, further comprising a conductor pattern contacting with said diffusion region and said gate electrode such that said conductor pattern extends [between said side wall oxide film and said first insulation film] along a surface of said side wall oxide film.

37. (Amended) A semiconductor device as claimed in claim [36] 34, further comprising [a] another silicide [layer] region formed selectively on a surface of said gate electrode.

38. (Amended) A semiconductor device, comprising:

a substrate;

a gate electrode provided on said substrate;

a diffusion region formed in said substrate adjacent to said gate electrode;

a side-wall insulation film formed on a side wall of said gate electrode; [and]

a self-aligned contact hole defined by said side-wall oxide film and exposing said diffusion region; and

a silicide region formed selectively on a surface of said diffusion region,

wherein said semiconductor device further includes:

a first insulation film provided on said gate electrode so as to cover said side wall oxide film partially;

a second insulation film having a composition different from a composition of said first insulation film and provided on said first insulation film;

an interlayer insulation film deposited on said second insulation film;

a contact hole formed in said interlayer insulation film, said contact hole extending through said first and second insulation films and exposing said self-aligned contact hole;

said first insulation film is formed of BPSG containing B with an amount of about 4 wt% or less.

39. (Amended) A semiconductor device as claimed in claim 38, further comprising a conductor pattern contacting with said diffusion region and said gate electrode such that said conductor pattern extends [between said side wall oxide film and said first insulation film] along a surface of said side wall oxide film.

41. (Amended) A semiconductor device as claimed in claim 40, further comprising [a] another silicide [layer] region formed selectively on a surface of said electrode.